A SEMICONDUCTOR DEVICE LAYOUT AND CHANNELING IMPLANT PROCESS

ABSTRACT

A device structure and method for forming graded junction using a implant process. Embodiments of the invention comprise implanting ions into said silicon substrate to form doped regions adjacent to said gate. The orientation of the channel region in the Si crystal structure (channel direction < 100>) in combination with the large angle tilt and twist implant process produce doped regions that have a more graded junction. The orientation and implant process creates more channeling of ions. The channeling of ions creates a more graded junction. When implemented on a HV MOS TX, the graded junction of the LDD increases the breakdown voltage. Another embodiment is a FET with an annular shaped channel region.